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01_Revision_History.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.1	RC00	2018-12	GW	- Bugfix	
2.0	RC00	2020-11	GF	- New sensing stucture; new TDSO footprint; bugfixes	
2.1	RC00	2021-03	GF	- Removed GND plane, satellite sensor configuration	
2.2	RC00	2021-07	GF	- Restored GND plane for better dI/dt immunity	
2.3	RC00	2021-10	GF	- Introduced LDO for better supply stability.	

TLE4972 TDSO16 StandardPCB S-Bend Evaluation Board

Default_Assembly

2.3

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10/2021

Link to Top Level Document

02 Top Level
02_Top_Level.SchDoc

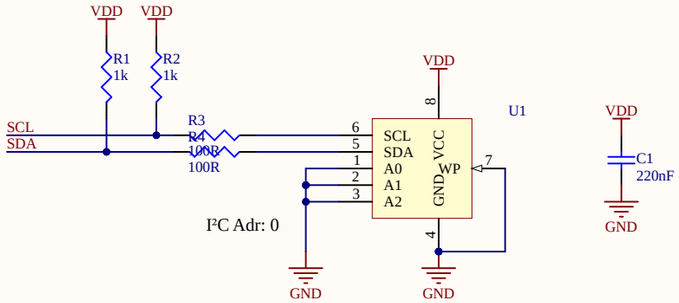
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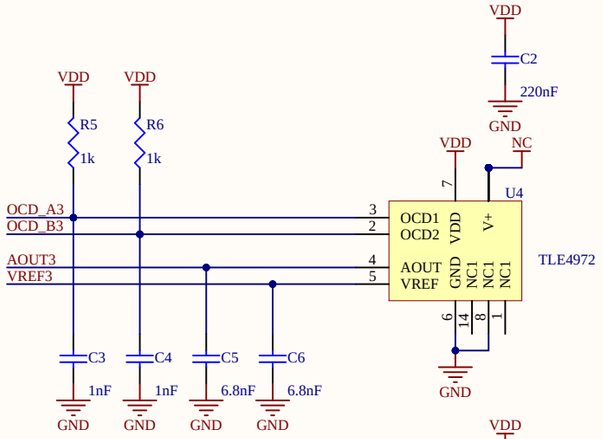
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Date: 11.10.2021	Time: 17:22:26	Author: GF	Sheet of 3

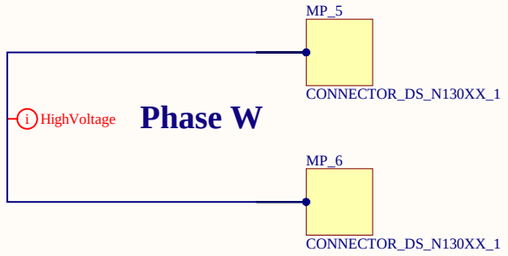
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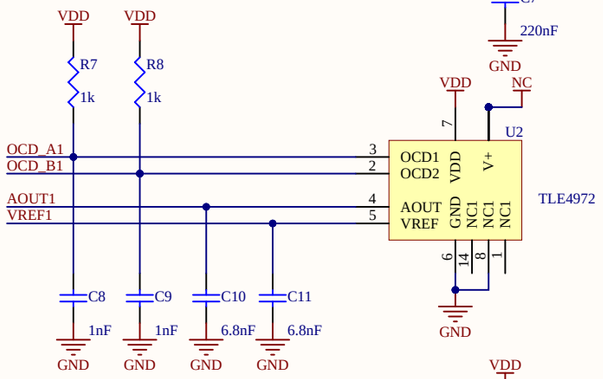
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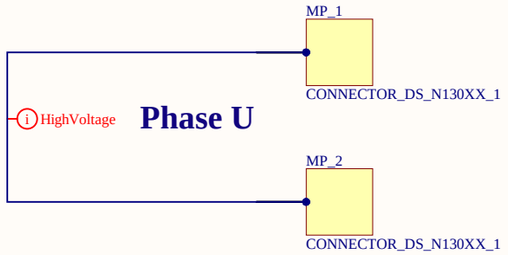


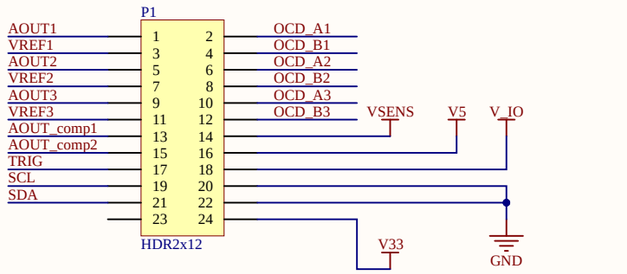
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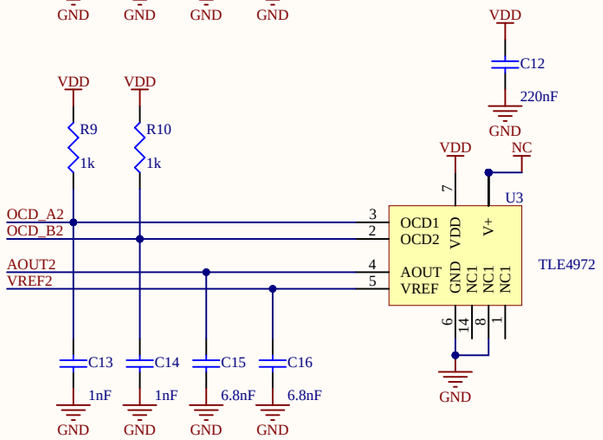


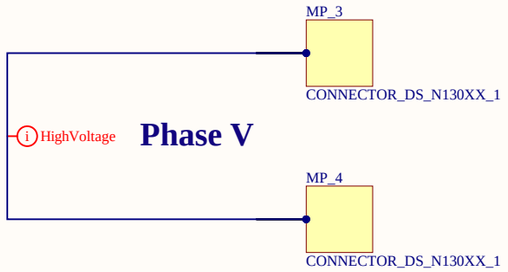


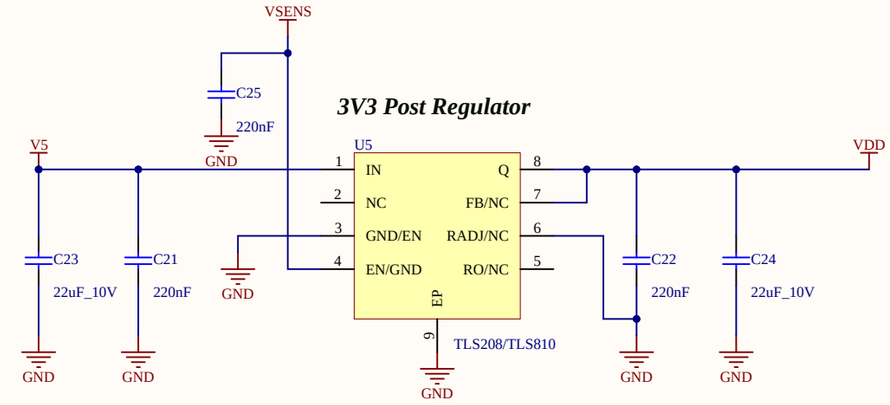


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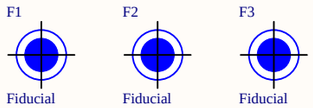


Miscellaneous
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Miscellaneous.SchDoc



BOM Report Configuration

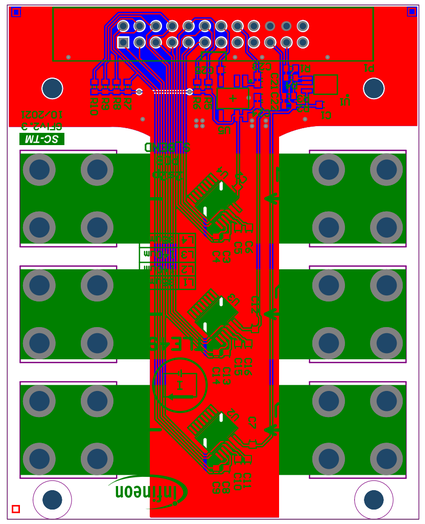


Note!
This component is used to define BOM report configuration.
If this component is deleted before other components from database are placed in this project, the BOM report configuration gets lost!

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Size: A3	Document Name: Miscellaneous.SchDoc	Rel.	Rev. 2.3
Date: 11.10.2021	Time: 17:22:27	Author: GF	Sheet of 3

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Layer	Name	Material	Thickness	Constant	Board Layer Stack	
	Top Overlay					
	Top Solder	Solder Resist	0.020mm	3.5		
1	L1_Top	copper	0.035mm			
	Prepreg1	FR4	0.115mm	4.6		
	Prepreg2	FR4	0.115mm	4.6		
2	L2_Middle	copper	0.140mm			
	Core	FR4	0.700mm	4.6		
3	L3_Middle	copper	0.140mm			
	Prepreg3	FR4	0.115mm	4.6		
	Prepreg4	FR4	0.115mm	4.6		
4	L4_Bottom	copper	0.035mm			
	Bottom Solder	Solder Resist	0.020mm	3.5		
	Bottom Overlay					

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PCB DESIGNER: GF			
DATE: 11.10.2021	PART NO.:	REL.: <Rel>	REV.: <Rev>
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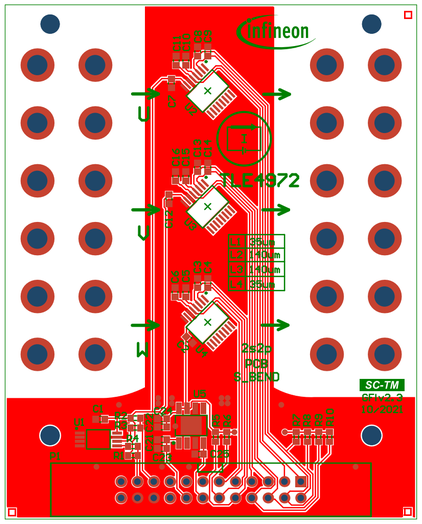
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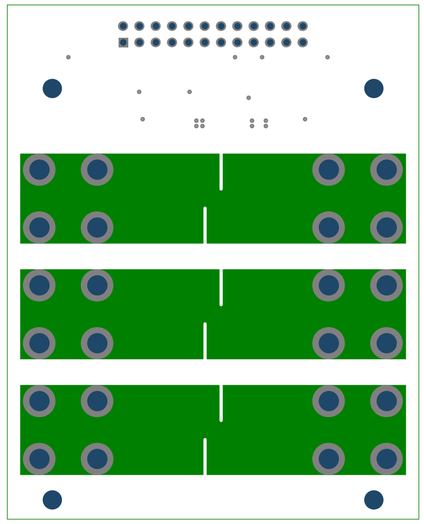
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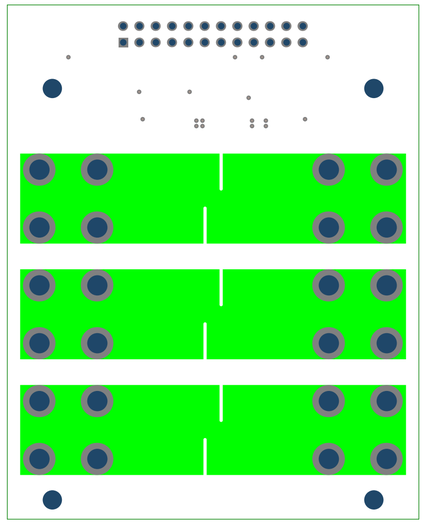
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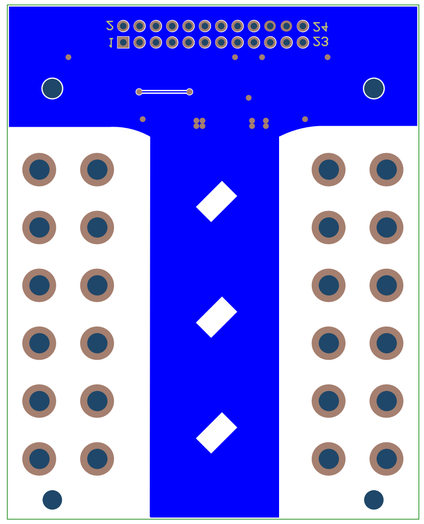


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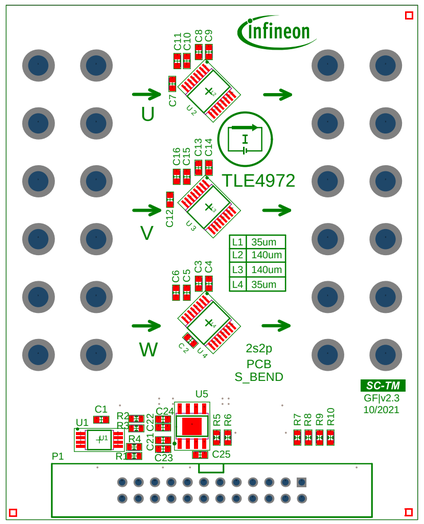




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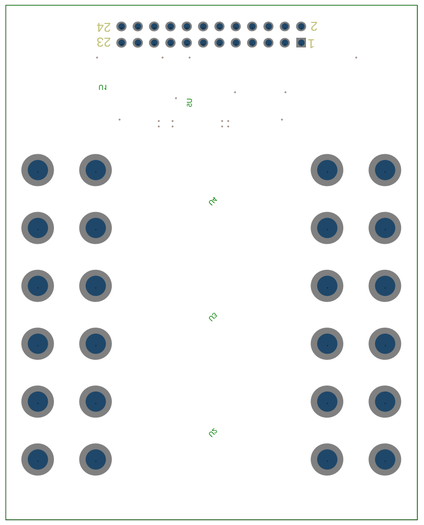
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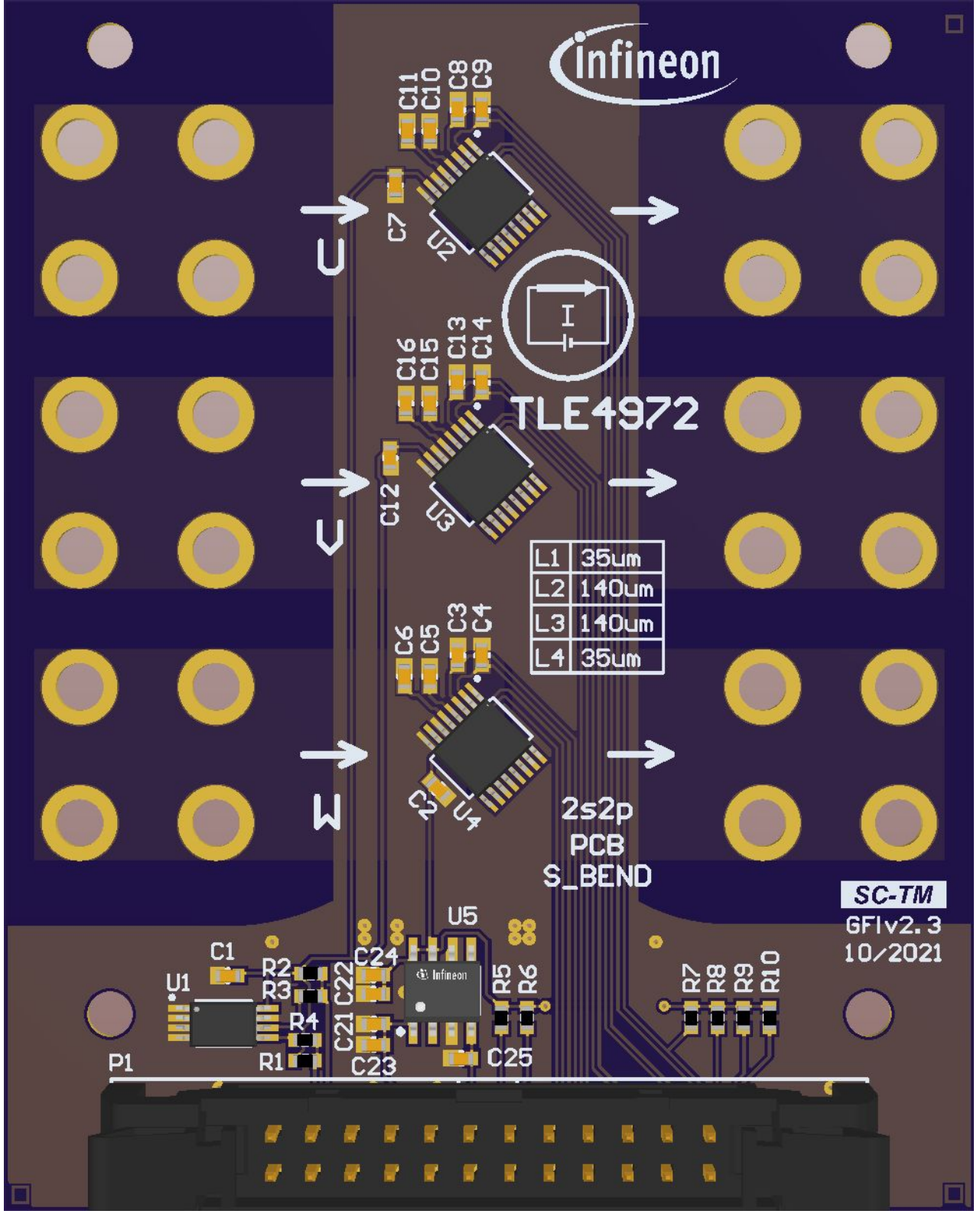
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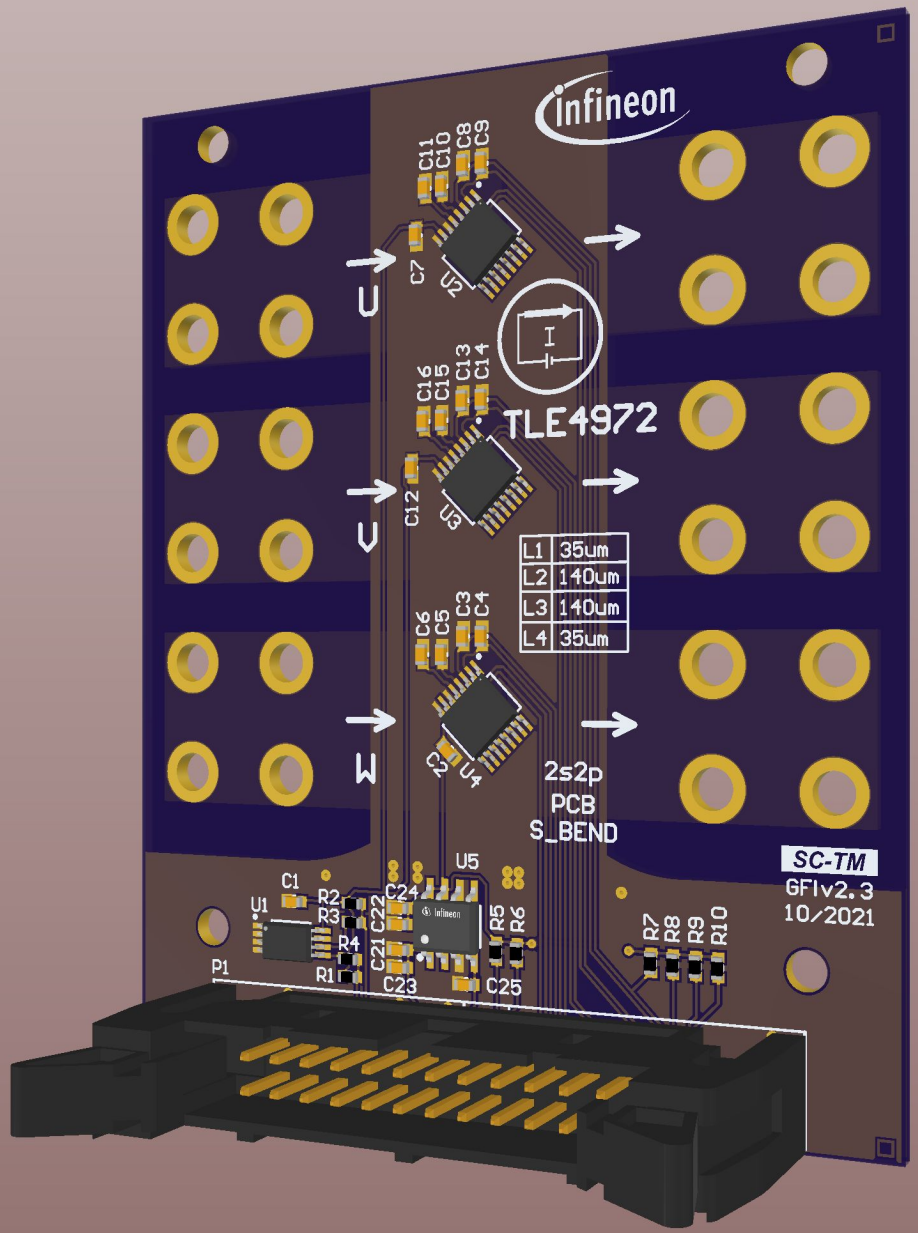


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TLE4972
U1
U2
U3
U4
U5
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
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L2 140um
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S_BEND
SC-TM
GFIv2.3
10/2021


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